

BOS Meeting - I

Date : 8/5/2018

Head of the department convened the meeting of Board of studies members in board room at 10:00 Am on 8th may 2018. to discuss about B.Tech and M.Tech Course structures & syllabus that to be commenced from academic year 2018-19 under autonomous syllabus system.

Agenda for the meeting.

1. TO welcome the BOS members
2. TO review the Ad-hoc BOS meeting held on 1st may 2018
3. TO discuss, review and approve the proposed curriculum commencing from Academic year 2018-19 for B.Tech in ECE for the autonomous system.
4. TO discuss, review and approve the proposed curriculum in ECE for M.Tech in Communication Engineering from the academic year 2018-19
5. TO discuss, review and approve the proposed curriculum in ECE for M.Tech in VLSI Design & Embedded Systems for autonomous system commencing from the academic year 2018-19
6. Any other matter with the permission of the chair

Minutes of meeting:

Agenda 1: TO welcome the BOS members

Resolution 1: Head of the department as the chair of the meeting, invited all the Board of studies members.

Agenda 2: To review the Ad-hoc BOS meeting held on 1st May 2018.

Resolution 2: The members of BOS reviewed the Ad-hoc BOS meeting resolutions held on 1st May 2018.

Agenda 3: To discuss, review and approve the proposed curriculum in ECE for B.Tech for the autonomous system commencing from the academic year 2018-19.

Resolution 3: The chair has presented the AICTE and proposed course structures and curriculum in ECE for B.Tech for autonomous system. The chair has discussed about enhancements made in the curriculum. Committee members suggested the following.

1. Suggested to reduce special semiconductor diodes in unit 2, and if possible move the concepts like photo diodes and PIN diodes to optical communication. Also suggested to reduce the no. of contact hour for unit-1 of Electronic Devices Course in III semester.

2. For III semester Courses signals & systems and probability & stochastic processes, taught these courses using matlab.

3. For the EDC Lab suggested to separate Halfwave and Fullwave rectifiers experiments, and combine the PN junction diode and Zener diode experiments.

4. For the mandatory course PDC include Time base Comptrols.

5. For IV semester course electromagnetic waves and Transmission Lines, include review of electromagnetic fundamentals, and split EM wave characteristics unit.
6. For IV semester Analog communication course reduce concept of amplitude modulation; remove radio receiver chapter if possible.
7. For AC Laboratory, include ICs for modulation experiments (DSB-SC) and perform application oriented experiments like FM using PLL.
8. Include design experiments for Electronics circuits lab and use P-SPICE software.
9. Include courses offered by other departments for open electives and finalized by discussing with all HODs.
10. Allot one faculty for coordinating the MOOC course and allot contact hours.
11. For soft skills and personality development course to be taken as theory instead of laboratory.

Agenda 4: To discuss, review and approve the proposed curriculum in ECE for M.Tech in Communication Engineering & Signal processing for autonomous system commencing from the academic year 2018-19

Resolution 4: members suggested to change the titles of Communication system design using

DSP algorithms and wireless Broadband communication members also suggested that include signal representation of Gram Schmidt orthogonalization as a first unit in Advanced Digital Communication subject.

Include Basics of CMOS as a first unit in CMOS RF circuit design.

Also suggested to increase audio processing topics in Speech and Audio processing subject.

Agenda 5: TO discuss, review and approve the proposed curriculum in ECE for M.Tech in VLSI Design & Embedded Systems for the autonomous system commencing from the Academic year 2018-19.

Resolution 5: members are suggested following

1. To remove self learning course from III Semester.
2. In digital system synthesis and verification subject, most of the topics are on Verilog. So change the syllabus including synthesis and verification process concepts, verify the syllabus of Soc Design & Soc architecture if both are different then continue.

Agenda 6: Any other matter with permission of the chair.

Resolution 6: As per the AICTE model curriculum, it is finalized by limiting the no. of credits to 160 for UG and 64 for PG program.

The chair has expressed gratitude to the all the BOS members.

S. NO	Name	position	Signature
1.	Dr. T. J. V. S. Rao	chairman	TJV SL Rao
2.	Dr. U. Eranna	member	
3.	Dr. P. Srikasi Rao	member	PSR
4.	Dr. K. padma priya	member	K. padma priya 8/5/18
5.	Sri. G. mallikarjun Rao	member	G. mallikarjun Rao 8/5/18
6.	S. Adhi Sesku.	member	